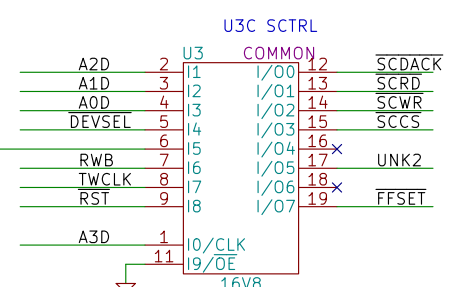
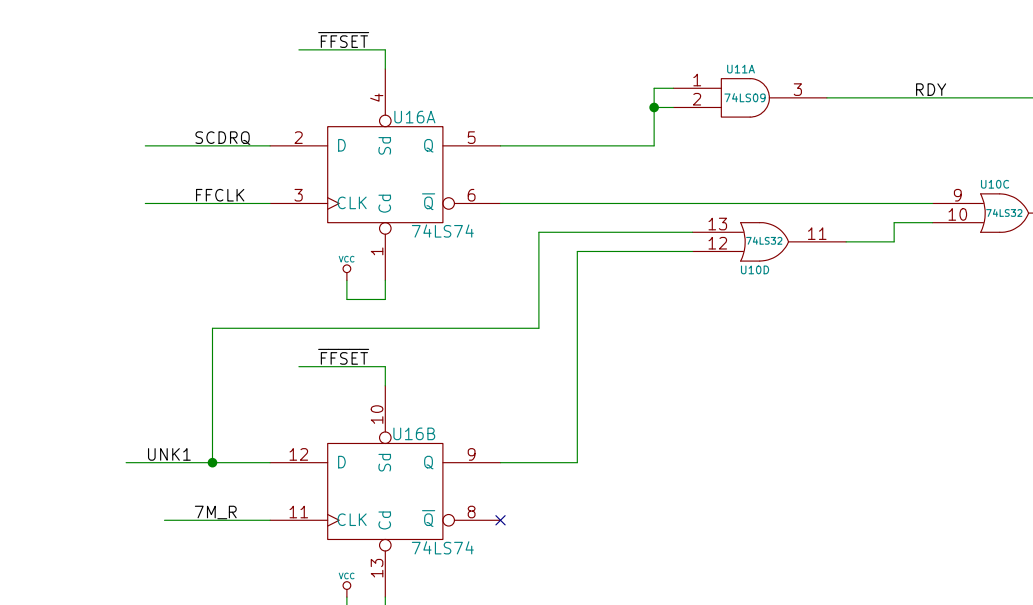
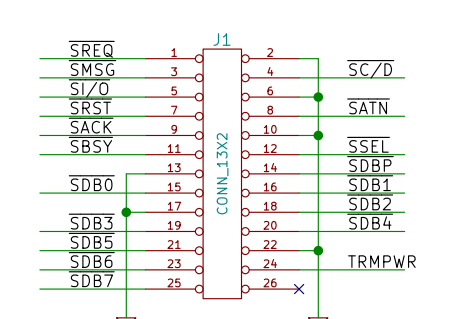
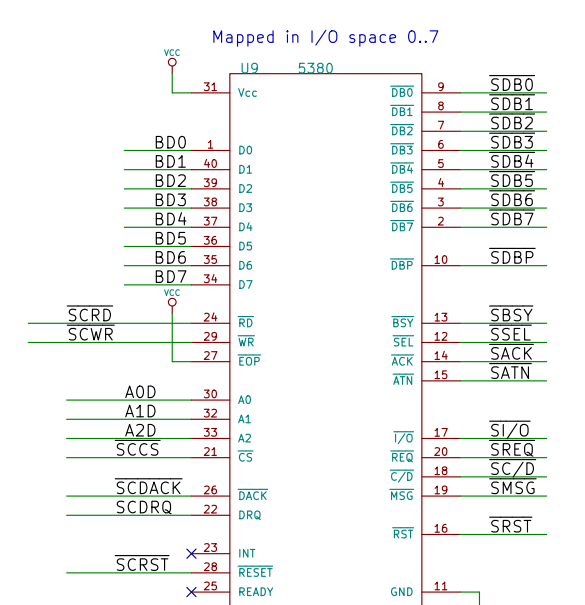
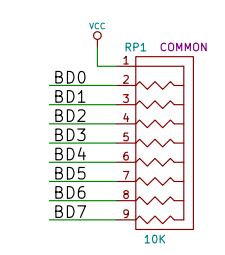
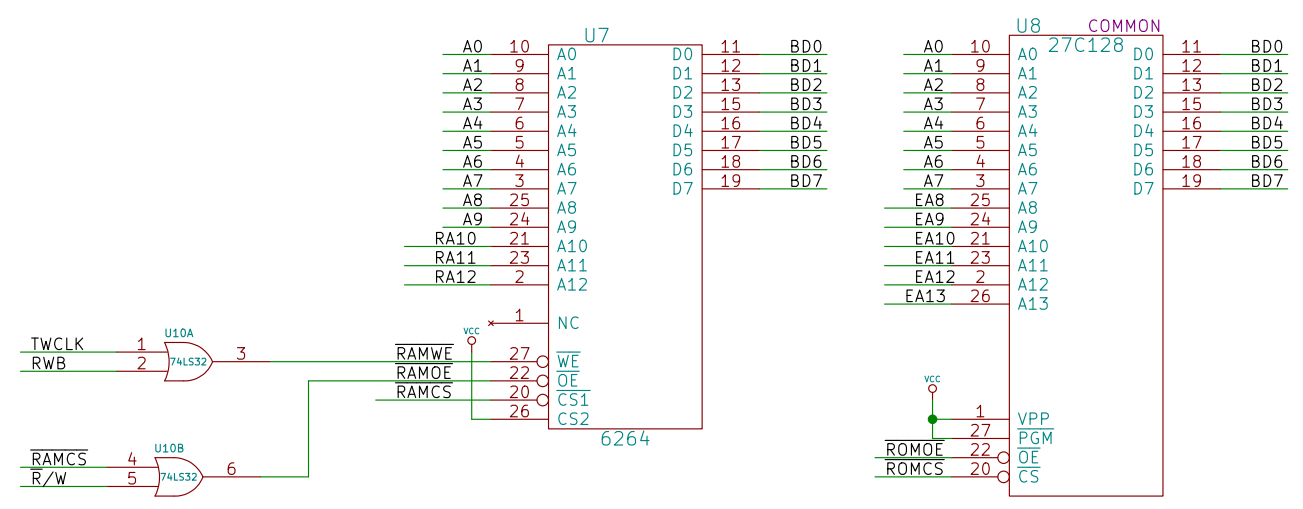
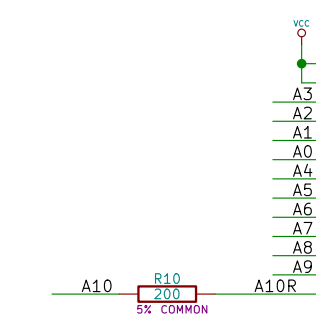


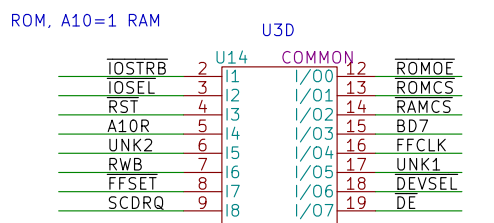
DEVSEL: 16 bytes I/O space at \$C0x0-\$C0xF (x=n+9)
 IOSEL: 256 bytes memory at \$Cn00-\$CnFF
 IOSTRB: 2K memory at \$C800-\$CFFF



SCCS = DEVSEL * IA3D
 SCRD = SCCS * RWB
 SCWR = TWCLK * RWB

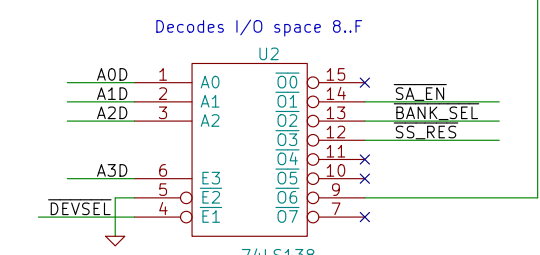


A10=0 ROM, A10=1 RAM

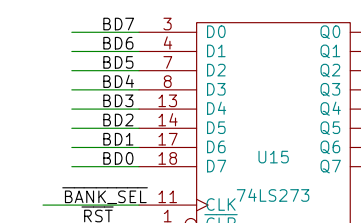
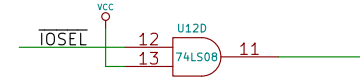
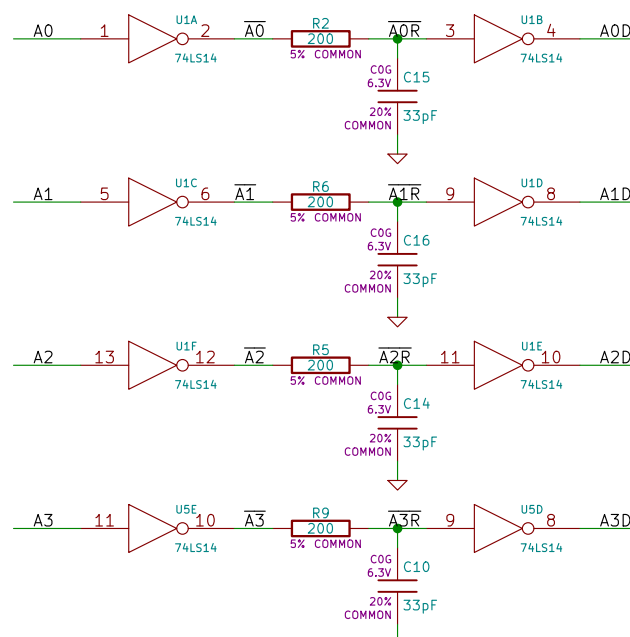
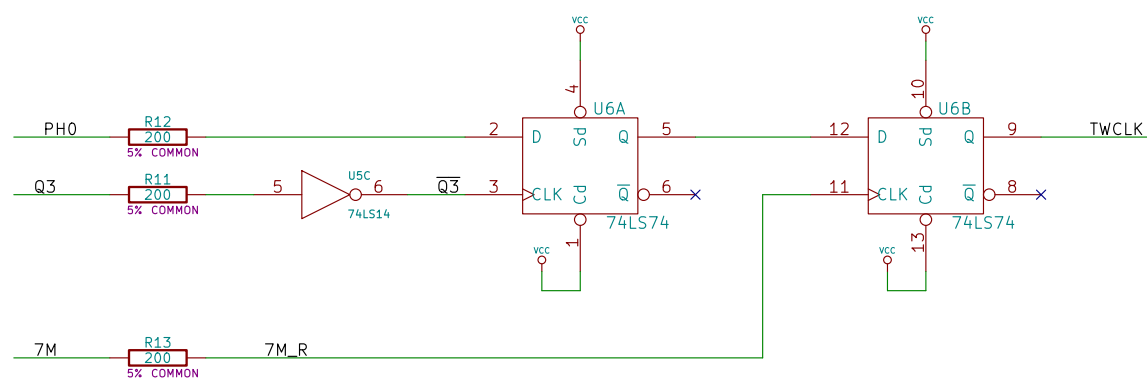


MEM ENABLE LATCH
 Set on IOSEL
 Reset on IOSTRB & ROM_DIS

ROMCS = MEM_EN * IOSTR * IA10R
 ROMOE = ROMCS * IRWB
 RAMCS = MEM_EN * IOSTR * A10R
 DE = DEVSEL + IOSEL + (IOSTR * MEM_EN)
 BD7_OE = DEVSEL * DRQ_EN * IRWB
 BD7 = SCDRQ



8: PDMA/DACK
 9: SCSI ID
 A: BANK SELECT
 B: Reset 5380
 C: RSVD
 D: PDMA Enable
 E: Read DRQ on D7
 F: RSVD



BANK REGISTER: bit 0..3 ROM Addr, 4..6 RAM Addr, 7 RSVD

